PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Keeth et all.

Serial No.: 08/530,661

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For: SEMICONDUCTOR MEMORY CIRCUITRY

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BRIEF ON APPEAL

Commissioner of Patents and Trademarks
Alexandria, VA 22313-1450

Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is submitted in TRIPLICATE pursuant to 37 C.F.R.§ 1.192(a) and in the format required by 37 C.F.R. § 1.192(c) and with the fee required by 37 C.F.R. § 1.17(c):

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(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., the assignee of the pending application as recorded at Reel 7671, Frame 0965 with the United States Patent and Trademark Office.

(2) RELATED APPEALS AND INTERFERENCES

Neither Appellant, Appellant's representative, nor Assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF CLAIMS

Claims 6-10, 18, 19, 22, 23, 25 and 26 are pending in the application.

Claims 1-5, 11-17, 20, 21, 24 and 27 have been previously withdrawn.

Claims 6-10, 18, 19, 22, 23, 25 and 26 stand rejected.

No claims are allowed.

The rejections of claims 6-10, 18, 19, 22, 23, 25 and 26 are being appealed.

(4) STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed on January 28, 2004. On April 2, 2004, the Applicants filed Remarks under 37 C.F.R. § 1.116 in response to the Examiner's remarks in the Final Office Action of January 28, 2004. No amendments were proposed in the Remarks. An Advisory Action mailed on April 13, 2004 found the Applicants' arguments in the Remarks unpersuasive and maintained the rejection of claims 6-10, 18, 19, 22, 23, 25 and 26.

(5) SUMMARY OF THE INVENTION

The invention presently claimed in pending claims 6-10, 18, 19, 22, 23, 25 and 26 relates to semiconductor memory fabrication at the 64M and 16M integration levels. (Specification, page 2, ¶ [0001]). Specifically, the invention presently claimed is a semiconductor memory device of smaller size or consumed monolithic die area than prior art devices. (Specification, page 23, ¶ [00117]).

In one embodiment of the present invention, a semiconductor memory device is provided that comprises a 16M semiconductor memory device with a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells occupying an area on a semiconductor die which is no greater than 14 mm^2. (Specification, page 25, ¶ [00124]). Redundant memory cells are provided. (Specification, page 23, ¶ [00118]). The 16M semiconductor memory device further comprises peripheral and pitch circuitry. (Specification, page 25, ¶ [00124]).

In another embodiment of the present invention, a 16M semiconductor memory device is provided that comprises a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells arranged into memory arrays on a semiconductor die. At least one of the memory arrays contains at least one area of 100 square microns of continuous die surface which is occupied by at least 128 of the functional and operably addressable memory cells. (*Id.*). Redundant memory cells are provided. (Specification, page 23, ¶ [00118]). Peripheral and pitch circuitry also exists on the semiconductor die, relative to the memory arrays. (Specification, page 25, ¶ [00124]).

In yet another embodiment of the present invention, a 64M semiconductor memory device is provided that comprises a total of no more than 68,000,000 functional and operably addressable memory cells arranged into memory arrays on a semiconductor die. (Specification, page 23, ¶ [00117]). At least one of the memory arrays contains at least one area of 100 square microns of continuous die surface which is occupied by at least 128 of the functional and operably addressable memory cells. (Specification, page 24, ¶ [00120]). Redundant memory cells are provided. (Specification, page 23, ¶ [00118]). Peripheral and pitch circuitry also exists on the semiconductor die, relative to the memory arrays. (Specification, page 24, ¶ [00120]).

(6) ISSUE

Whether claims 6-10, 18, 19, 22, 23, 25 and 26 are patentable under 35 U.S.C. § 103(a) over Takashima et al. (United States Patent No. 5,838,038) in view of Eimori (United States Patent No. 5,610,418), Nakamura et al. (United States Patent No. 5,654,577) and Takahashi et al. (United States Patent No. 5,287,000).

(7) GROUPING OF CLAIMS

Appellant submits that claims 6-10, 18 and 19 stand and fall together for purposes of this appeal. Appellant submits that support for the patentability of claims 6-10, 18 and 19 is set forth in Sections 8(C)(1)-(4). It is further submitted that claims 22, 23, 25 and 26 stand but do not fall with claims 6-10, 18 and 19, as they are separately patentable for the reasons set forth in Section 8(C)(5).

(8) ARGUMENT

A. Authorities Relied Upon

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations.

Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

It is improper to combine references where the references teach away from their combination. MPEP § 2145 (citing *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)).

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert.denied*, 469 U.S. 851 (1984).

The Federal Circuit has repeatedly cautioned against employing hindsight by using the applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teaching of the prior art. *See, e.g., Grain Processing Corp. v. American-Maize Prods. Co.*, 840 F.2d 902, 907, 5 U.S.P.Q.2d 1788, 1792 (Fed. Cir. 1988).

B. Summary of Cited Prior Art

Takashima et al. describes a semiconductor memory device with reduced-size memory cells. Each memory cell occupies an area of $6F^2$, where "F" is a minimum processing size. (Takashima, column 3, line 51). Takashima et al. also describes a four-level memory array (Takashima, figure 29) and a five-level memory array. (Takashima, figure 47). However, Takashima et al. does not describe features of the semiconductor memory device other than the memory cells and array. There is no description of either peripheral or pitch circuitry. Similarly,

memory cell array size and feature size are not disclosed.

Eimori describes a structure of a semiconductor memory device such as a capacitative element in a memory cell on a dynamic random access memory ("DRAM") device. (Eimori, column 4, line 55). The structure is designed according to a 0.25 μm design rule (Eimori, column 10, line 61), meaning that the minimum feature size of the structure is 0.25 μm. Application of a design rule does not imply that every feature within the structure is at the minimum size, as indicated by the dimensions shown in Figures 6 and 9.

Nakamura et al. describes a semiconductor integrated circuit device, and specifically refers to a 16M DRAM device. (Nakamura, column 4, line 26). Additionally, the device includes peripheral circuits such as an address buffer and a decoder, as well as redundancy circuits, signal control circuits and an internal voltage limiter. (Nakamura, column 4, lines 43-65). Means or methods to minimize the 16M DRAM device are not disclosed.

Takahashi et al. describes a DRAM where the die is encapsulated in a package with pins extending outwardly. (Takahashi, column 6, line 7).

C. Arguments for Patentability of Claims 6-10, 18, 19, 22, 23, 25 and 26

(1) *Claims 6 and 18 are patentable because the cited references do not teach or suggest all of the claim limitations.*

In rejecting claim 6, the Office asserts that Takashima et al. discloses a DRAM device where the cell size is $6F^2$, and that this feature may be combined with the 16M DRAM device disclosed by Nakamura et al. The Nakamura et al. DRAM device includes peripheral circuitry.

The Takashima et al. and Nakamura et al. combination is further combined by the Office with the packaged semiconductor die of Takahashi et al. to create a packaged DRAM device with peripheral circuitry and $6F^2$ memory cell size. Finally, Eimori's teachings of a 0.25 μm design rule implementation in a DRAM device are added to the combination to suggest a packaged DRAM device including peripheral circuitry and $6F^2$ memory cell size using a 0.25 μm design rule.

Similarly, in rejecting claim 18, the Office cites Takashima et al. in view of Eimori, Nakamura et al. and Takahashi et al. to assert a prior art packaged DRAM device including peripheral circuitry and $6F^2$ memory cell size using a 0.25 μm design rule as evidence that memory cells may exist at a high density on a semiconductor die.

Claims 6 and 18, however, are patentable because the combination of Takashima et al. in view of Eimori, Nakamura et al. and Takahashi et al. by the Office does not teach or suggest all the claim limitations. Specifically, claim 6 limits the occupied area of "from 16,000,000 to 17,000,000 functional and operably addressable memory cells" to a total area no greater than 14 mm^2. Claim 18 limits the occupied density to 128 functional and operably addressable memory cells per 100 μm^2 on a semiconductor die. These limitations are not taught by the cited references.

The Office asserts that a device manufactured according to a 0.25 μm design rule containing some 16,000,000 to 17,000,000 memory cells of area $6F^2$ should only occupy an area of less than 6 mm^2. Or, in terms of density, the Office asserts that a design rule of 0.25 μm will result in a density of 270 memory cells per 100 μm^2 on a semiconductor die. This is in error,

reflecting a misapplication of the term "design rule." A design rule refers to a minimum feature size. A device manufactured according to a 0.25 μm design rule will include features that are only 0.25 μm in width. However, because the design rule is only a minimum, many features on the device will have larger dimensions. For example, figures 6 and 9 of Eimori, relied upon by the Office, show multiple feature dimensions. Thus, the area occupied by 16,000,000 to 17,000,000 memory cells of size $6F^2$ each where "F" equals 0.25 μm is greater than the result of 17,000,000 x 6 x (0.25 μm)^2. In other words, the occupied area must be greater than the 6 mm^2 asserted by the Office. Likewise, the density must be less than 1/(6 x (0.25 μm)^2), or 2.7 cells per μm^2 asserted by the Office.

Furthermore, a memory device containing "from 16,000,000 to 17,000,000 *functional and operably addressed* memory cells" will actually include a far greater number of memory cells. In accordance with standard semiconductor memory fabrication, a semiconductor memory device is designed to include additional redundant memory cells that may be operably fused to replace inoperable memory cells created during fabrication. "Where an inoperable memory cell is determined during tests, the entire respective row (word line) or column (bit line) is fused out of operation, and a substitute operable redundant row or column substituted its place." (Specification, page 23, ¶ [00118]). The result is that a semiconductor memory device will include substantially more memory cells than the total operable memory cells of the finished memory device.

Thus, the combination of Takashima et al. in view of Eimori, Nakamura et al. and Takahashi et al. cannot be relied upon to teach or suggest a specific die area occupied by a certain

number of *functional* memory cells.

(2) Claims 6 and 18 are further patentable because the claimed invention reflects a desired but hitherto unrealized improvement on existing technology.

Claims 6 and 18 are further patentable because the claimed invention is highly sought after, but not yet realized by others as of the invention's filing date. "Existence of [a] defect creates a demand for its correction, and it is reasonable to infer that the defect would not persist were the solution 'obvious.'" *In re Fielder*, 471 F.2d. 640, 644 (CCPA 1973) (citing "Subtests of 'Nonobviousness': A Nontechnical Approach to Patent Validity," 112 U. Pa. L. Rev. 1169, 1172 (1964)). Also, "[t]he existence of an enduring, unmet need is strong evidence that the invention is novel, not obvious, and not anticipated. If people are clamoring for a solution, and the best minds do not find it for years, that is practical evidence . . . of the state of knowledge." *In re Mahurkar Patent Litigation*, 831 F. Supp. 1354, 1377-78 (N.D. Ill. 1993). In the present invention, the long-sought goal has been the maximized density of single transistor and other memory cells in semiconductor memory fabrication." (Specification, page 2, ¶ [0005]). Claims 6 and 18 are to a memory device with hitherto unrealized memory cell densities. The fact that such a device had not previously been invented is evidence of non-obviousness.

One reason that such a device had not previously been invented is because of the inherent difficulties of shrinking a memory cell *and* related circuitry. Shrinkage of a memory cell, whether $8F^2$ or $6F^2$, to a memory cell pitch of less than 1 μm involves a number of significant problems. (Specification, page 6, ¶ [0046]). For example, as the minimum pitch falls below 1.0 μm,

conventional "LOCal Oxidation of exposed Silicon" ("LOCOS") techniques fail due to excessive encroachment of the oxide beneath the masking stack (*Id.*). Furthermore, the memory cell storage node capacitance tends to decrease with the decrease in cell size, yet a minimum storage capacity for stored charge is required to maintain reliable operation. (Specification, page 7, ¶ [0048]). As yet another example of scaling issues, adequate spacing is required between adjacent devices, such as between a bit line contact and construction of a capacitor. (Specification, page 14, ¶ [0078]). Furthermore, field oxide regions, such as field oxide that is used to provide electrical isolation between certain adjacent banks of memory cells within an array, need to be eliminated to reduce size. (Specification, page 18, ¶ 0094]).

Additionally, bit line circuitry and bit line spacing affect the feasibility of shrinking an individual memory cell design within an array to a $6F^2$ size. (Specification, page 19, ¶ [0097]). Furthermore, the space consumed by the digit lines D and D* and their associated circuitry become one of the limiting factors for conversion to a $6F^2$ size. (*Id.*). All of the aforementioned design considerations would need to be addressed in order for the memory cell as disclosed by Takashima et al. to be shrunk to a size resulting in the densities as claimed in independent claim 6. As a further example, the memory cell of Takashima as illustrated in Figure 28, includes LOCOS isolation, illustrated as oxide 133 under the word lines and between adjacent memory cells, with spacing also illustrated between bit line contacts and storage nodes. A simple reduction in the photolithographic feature size, if even possible, would result in the problems that are identified and addressed only by the invention presently claimed.

The Office asserts that it is obvious to combine the reduced-size memory cell of

Takashima et al. with the design rule applied in Eimori to achieve memory area commensurate with that in claim 6. However, because of the many explained difficulties associated with shrinking a memory device, the asserted combination does not teach sufficient detail to enable a combination of the references to establish a *prima facie* case of obviousness regarding the claimed invention.

(3) Claims 7-10 are each allowable, among other reasons, as depending either directly or indirectly from claim 6, which is allowable.

Claims 7-10 are each allowable, among other reasons, as depending either directly or indirectly from claim 6, which is allowable. In effect, the cited references do not teach or suggest all of the claim limitations.

(4) Claim19 is allowable, among other reasons, as depending either directly or indirectly from claim 18, which is allowable.

Claim 19 is allowable, among other reasons, as depending either directly or indirectly from claim 18, which is allowable. In effect, the cited references do not teach or suggest all of the claim limitations.

(5) Claims 22, 23, 25 and 26 are allowable because the cited references do not teach or suggest all of the claim limitations.

Claims 22, 23, 25 and 26 are allowable because the cited references do not teach or suggest all of the claim limitations. The Office asserts, with respect to claims 22, 23 and 26, that "the 16M device has no more than 68M memory cells and with the density shown will have 270 devices in 100 μm^2." (Final Office Action, page 3). Also, with respect to claim 25, the Office

asserts that "the memory arrays with the density shown will have 270 devices in 100 μm^2." The Office once again relies on Takashima et al. in view of Eimori, Nakamura et al. and Takahashi et al. to assert a prior art 16M packaged DRAM device including peripheral circuitry and $6F^2$ memory cell size using a 0.25 μm design rule as evidence that memory cells may exist at a high density on a semiconductor die. However, the assertion of the combined references as obviating prior art is in error.

First, the referenced prior art asserts a 16M DRAM device. (Nakamura, column 4, line 26). Claims 22, 23, 25 and 26 refer to a device comprising of "no more than 68,000,000 functional and operably addressable memory cells." In other words, the referenced semiconductor memory device is a 64M device, not a 16M device. (Specification, page 23, ¶ [00117]). Thus, the combined references clearly do not teach or suggest all of the claim limitations in independent claim 22. Independent claim 22, then, is allowable.

Dependent claims 23, 25 and 26 are each allowable, among other reasons, as depending either directly or indirectly from claim 22, which is allowable. In effect, the cited references do not teach or suggest all of the claim limitations.

Furthermore, for the same reasons that make claims 6 and 18 allowable, claim 22 is allowable because the cited references do not offer an enabling density of functional memory cells on the semiconductor die, nor do the cited references suggest means to shrink both the memory cells and accompanying circuitry so as to overcome the problems traditionally associated with high density memory arrays, as previously stated. Finally, because a design rule refers only to a minimum feature size, and because far more memory cells than the desired

number of functional memory cells must be fabricated in order to achieve a specified density of functional memory cells, the number of functional memory cells on a 100 μm^2 area on a semiconductor die will be far less than the result of $100/(6*F^2)$, as the Office asserts when stating that 270 memory cells may exist in a 100 μm^2 area.

Once again, dependent claims 23, 25 and 26 are each allowable, among other reasons, as depending either directly or indirectly from claim 22, which is allowable. In effect, the cited references do not teach or suggest all of the claim limitations.

In view of the foregoing, Appellant respectfully submits that claims 6-10, 18, 19, 22, 23, 25 and 26 are allowable over Takashima et al. in view of Eimori, Nakamura et al. and Takahashi et al. and requests that the present rejections be withdrawn.

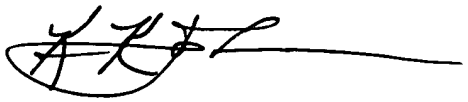
(9) APPENDICES

A copy of claims 6-10, 18, 19, 22, 23, 25 and 26 is appended hereto as "Appendix A."

(10) CONCLUSION

Appellant respectfully requests the reversal of the rejections of currently pending claims 6-10, 18, 19, 22, 23, 25 and 26 for the reasons set forth above.

Respectfully submitted,



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APPENDIX A

1. (Withdrawn) A 64M semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 64,000,000 to 68,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die the individual functional and operably addressable memory cells occupying area on the die within the memory arrays, the occupied area of all functional and addressable memory cells on the die having a total combined area which is no greater than 53 mm^2; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

2. (Withdrawn) The semiconductor memory device of claim 1 wherein the die is fabricated to include a total of four or less composite conductive line layers.

3. (Withdrawn) The semiconductor memory device of claim 1 wherein the peripheral circuitry, the pitch circuitry and the memory arrays have a total combined continuous surface area on the die which is less than or equal to 106 mm^2.

4. (Withdrawn) The semiconductor memory device of claim 1 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers, the occupied area of all functional and operable memory cells on the die having a total combined area on the die which is no greater than 40 mm^2.

5. (Withdrawn) The semiconductor memory device of claim 1 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers; the peripheral circuitry, the pitch circuitry and the memory arrays having a total combined continuous surface area on the die which is less than or equal to 93 mm^2.

6. (Previously presented) A semiconductor device including a memory, the semiconductor device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, the individual functional and operably addressable memory cells occupying area on the die within the memory arrays, the occupied area of all functional and addressable memory cells on the die having a total combined area which is no greater than 14 mm^2; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

7. (Previously presented) The semiconductor device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include a total of four or less conductive line layers.

8. (Previously presented) The semiconductor device of claim 6 wherein the peripheral circuitry, the pitch circuitry and the memory arrays have a total combined continuous surface area on the die which is less than or equal to 35 mm^2.

9. (Previously presented) The semiconductor device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five conductive line layers, the occupied area of all functional and operable memory cells on the die having a total combined area on the die which is no greater than 11 mm^2.

10. (Previously presented) The semiconductor device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five conductive line layers; the peripheral circuitry, the pitch circuitry and the memory arrays having a total combined continuous surface area on the die which is less than or equal to 32 mm^2.

11. (Withdrawn) A 4M semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 4,000,000 to 4,500,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, the individual functional and operably addressable memory cells occupying area on the die within the memory arrays, the occupied area of all functional and addressable memory cells on the die having a total combined area which is no greater than 3.3 mm^2; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

12. (Withdrawn) The semiconductor memory device of claim 11 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include a total of

four or less composite conductive line layers.

13. (Withdrawn) The semiconductor memory device of claim 11 wherein the peripheral circuitry, the pitch circuitry and the memory arrays have a total combined continuous surface area on the die which is less than or equal to 11.0 mm^2.

14. (Withdrawn) The semiconductor memory device of claim 11 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers, the occupied area of all functional and operable memory cells on the die having a total combined area on the die which is no greater than 2.5 mm^2.

15. (Withdrawn) The semiconductor memory device of claim 11 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers; the peripheral circuitry, the pitch circuitry and the memory arrays having a total combined continuous surface area on the die which is less than or equal to 10.2 mm^2.

16. (Withdrawn) A 64M semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 64,000,000 to 68,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable

memory cells of the memory arrays.

17. (Withdrawn) The semiconductor memory device of claim 16 wherein at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 170 of the functional and operably addressable memory cells.

18. (Previously presented) A semiconductor device including a memory, the semiconductor device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

19. (Previously presented) The semiconductor device of claim 18 wherein at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area has at least 170 of the functional and operably addressable memory cells.

20. (Withdrawn) A 4M semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 4,000,000 to 4,500,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

21. (Withdrawn) The semiconductor memory device of claim 20 wherein at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 170 of the functional and operably addressable memory cells.

22. (Previously presented) A semiconductor device including a memory, the semiconductor device comprising:

a total of no more than 68,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on a semiconductor die; and

circuitry formed on the semiconductor die permitting data to be written to and read from one or more of the memory cells, at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells.

23. (Previously presented) The semiconductor device of claim 22 wherein the total number of functional and operably addressable memory cells on the semiconductor die is no more than 17,000,000.

24. (Withdrawn) The semiconductor memory device of claim 22 wherein the total number of functional and operably addressable memory cells on the semiconductor die is no more than 4,500,000.

25. (Previously presented) The semiconductor device of claim 22 wherein at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area has at least 170 of the functional and operably addressable memory cells.

26. (Previously presented) The semiconductor device of claim 22 wherein at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area has at least 170 of the functional and operably addressable memory cells, and the total number of functional and operably addressable memory cells on the semiconductor die is no more than 17,000,000.

27. (Withdrawn) The semiconductor memory device of claim 22 wherein at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 170 of the functional and operably addressable memory cells, and the total number of functional and operably addressable memory cells on the semiconductor die is no more than 4,500,000.